1/4 inch 2Mega CMOS Image Sensor Fabrication

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Abstract

We fabricate a 1/4inch 2mega CMOS image sensor with the non-shared type 2.25um pixel with 4 transistors. To implement this pixel, we use borderless contact to connect driver transistor (Dx) and floating diffusion (FD). The borderless contact replaces one metal connection line and one metal1 contact so that we can ensure the optical fill factor for incident light. Also, this borderless contact helps to get similar fill factor with that of shared type pixels for the implementing 2.25um pixel. This paper presents another approach of pixel design and its competitive performance like 34% fill factor, 550mv saturation level and 10mV/sec dark current level.

1. Introduction

The progress of CMOS fabrication technology has reduced the pixel size in CMOS image sensors significantly, down to 2.2 x 2.2 um^2 [1]. However, most of companies face the similar problems like small fill factor and small light incident windows when they design small size pixels which have non-shared type pixels [2]. These problems are more critical if they want to realize the small size pixel with 4 transistor type or pinned photo diode type pixel [3]. So, most of companies use shared type pixels like 2 shared type or 4 shared type to implement 2.25um pixel or under 2.25um pixel [4].

However, shared type pixels have some issues which are not severe in the case of non shared type pixels. Shared type pixels are weak to the crosstalk because of its different space between photo diodes of shared pixel structure. This structure causes a pixel variation and results in maze noise. Especially, this maze noise is more critical at corner area of pixel array because of large incident angle.

If the spaces between photo diodes are equal, optical crosstalk and electrical crosstalk will happen the same amount in each pixel so there are small maze noises. So, companies need to consider design and process symmetries carefully [5].

In this paper, 2.25um non-shared type pixel structure is presented as an approach to reduce crosstalk and the characteristics of 2 Mega CMOS image sensor, which has the same pixel, is discussed.

2. Pixel architecture and borderless contact

1) Pixel architecture

Fig. 1 shows the pixel design architecture of this work, the most critical issue is to guarantee the optical fill factor for incident light by reducing inter-connection lines which comprises an pixel array, i.e. Tx, Rx, Sx, Vdd, Vout and Dx to FD in pixel array interconnection line. Except Dx to FD interconnection line, other lines cross the whole pixel area to connect the each pixel. However, Dx to FD inter-connection line is just to transfer the potential of FD to the gate of Dx and there is a little need for low resistivity but stable connection.

We use the borderless contact for the interconnection line, which is a standard process for normal logic or SRAM to maximize inter-connection routing efficiency [6]. For the borderless contact, the gate of Dx is extended to the floating diffusion so the interconnection line is replaced by the Dx gate poly. Also, there are no needs to make Dx gate contact. Eventually, the borderless contact is able to reduce 1 metal line and 1 metal1 contact. In Table 1, we compare the numbers of composition units for various pixel types.

Fig. 1 illustrates the circuit diagram of this work. To get the design advantage, the Dx Tr. gate of left side pixel is drawn to the FD junction of right side pixel and the gate poly and FD junction is connected by borderless contact. So, the pixel of this work uses the source follower of the left side pixel.

component	Type A	Type B	Type C	Type D
Transistor	4	4	2.5	1.75
Metal line	6	5	3	2
Metal1 CT	7	6	4	2.5

Table. 1. Comparison table of components of unit pixel

for each different pixel. Type A: Normal 4T pixel, Type B: Normal 4T pixel with borderless contact, Type C: 2Shared 4T pixel, Type D: 4Shared 4T pixel.

The other conditions except using the borderless contact and the source follower of the left side pixel are the same as normal 4T pixel. By developing a 2 mega pixel image sensor with the explained pixel structure using a 0.13um CMOS process, we can get 40% optical fill factor and 34% fill factor.

2) Borderless contact

Fig. 2 shows the top view design of borderless contact and its cross section SEM view. The size of borderless contact is 2times larger than normal contact size in Y direction to realize the stable connection between Dx and FD node.

The test structure of borderless contact is that the poly connected the each active over the field oxide with 0.1um active overlap and the borderless contact connected the poly and active.

The total borderless contacts in this test pattern are 5,000ea. The resistance of each borderless contact is 710ohm/ea. When the Dx gate and FD region are connected with metal line, the FD contact resistance is 50ohm and Dx gate contact resistance is 360ohm/ea because salicide process is not applied to the whole pixel area. It means that borderless contact resistance is 300ohm/ea larger than normal separated FD and Dx gate contact resistance. To verify the contact resistance of borderless contact itself, it is measured in Kelvin pattern. In that case, the contact resistance is 150ohm/ea for borderless contact. So, non-silicide poly and active sheet resistance contribute to the larger borderless contact Rc.

From these results, we reach the conclusion that borderless contact does not make high contact resistance. Also, the borderless contact transfers the potential from FD to Dx gate perfectly even in high poly sheet resistance because there are no current paths to the silicon substrate. Fig. 3 shows the comparison results of unit contact resistance which are used in this work.

3. Process integration and microlens shift

This work is processed in Dong Bu Electronics, which is a foundry company in Korea, with 0.13um technology. Basic process scheme and design rule are the same as normal logic 0.13um technology except the process for making photo diode. STI process is applied to separate active region. STI process can cause the dark current in photo diode because of its rough interface state between silicon and oxide. Appropriate thermal budget is controlled to minimize the dark current caused at interface state. Also, Co-salicide process is blocked for whole pixel area due to two reasons. First is to minimize dark current caused by metallic contaminations even which is not on photo diode. Second is to remove the salicide layer in photo diode area which blocks the incident light into photo diode. USG oxide was applied for IMD and IMO material.

The total height from silicon surface to the bottom of color filter is 3.0um. In the case of color filter, the height was 0.8um for Green filter. So, the total stack height from silicon surface to the bottom of Microlens was 3.8um. According to the simulation and experiment results, the appropriate microlens height is decided to focus the incident light into the photo diode.

In the case of 2Mega product, the incident angle of module lens reaches to 27 deg at 0.8 image field. So, it is very difficult to shrink the microlens with linear method. We applied a non-linear microlens shift for this work. According to the data, Gr/Gb ratio is in max 2% difference in all image area. Fig. 4. shows the captured white image and its Gr/Gb ratio in 64 divided area. There are no maze noises in all image area. Proper microlens shift and non-shared type pixel design minimize crosstalk which can make maze noise.

4. Sensor characteristics

By using the borderless contact to get proper optical fill factor and fill factor, we can make 2Mega CMOS image sensor with 2.25um pixel which is 4T non-shared pinned photo diode type.

According to the pixel design, optical fill factor and fill factor are 40% and 34% each. Measured performance of this work is given by Table 2. Fig. 5. shows the sample image of this work.

Parameters	Value	Remark
Pixel size	2.25 x 2.25 um^2	
Max. SNR	36 dB	
Dynamic Range	60.2dB	
Dark current	10mV/sec	
Sensitivity	750mV/lux sec	@Green
Saturation	> 550mV	

Table 2. Measured image sensor performances

5. Conclusion

2 Mega CMOS image sensor with non-shared pinned photo diode type is fabricated with 0.13um technology. Through this work, we can reach the below conclusions.
1) We can get 40% optical fill factor and 34% fill factor by using borderless contact at 2.25um 4T pinned photo diode structure.
2) According to the evaluation results of electrical characteristics of the borderless contact, it has process reliability to do mass production.
3) Non shared type pixel design and proper non-linear microlens shift reduce optical crosstalk. The Gr/Gb differences are less than 2% in all image area.
4) Saturation level is 550mV and dark level is 10mV/sec.

References

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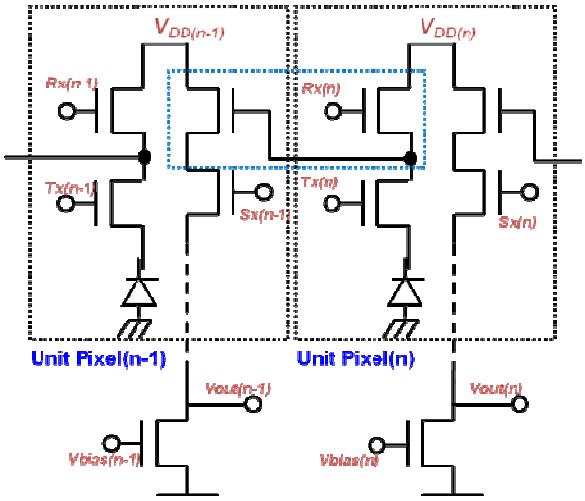
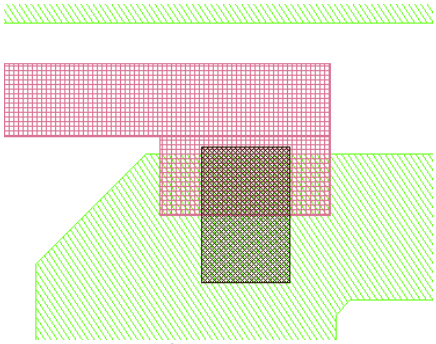
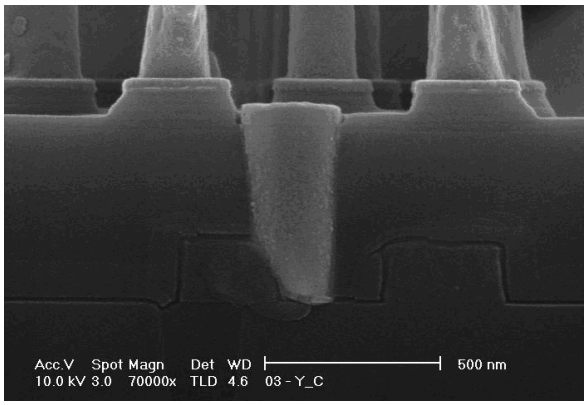


Fig. 1. Pixel architecture of this work. Pixel uses the source follower of left side pixel for the design advantage.



(a) Top view design of borderless contact



(b) Cross-Section SEM view of borderless contact

Fig. 2. Feature of borderless contact of this work.

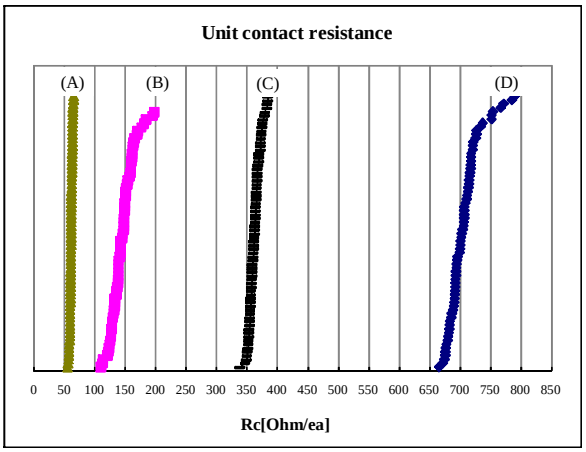
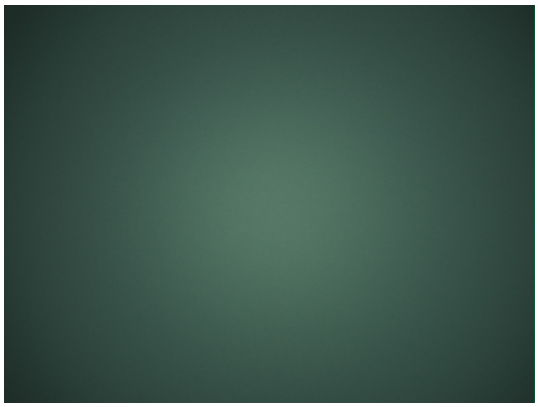


Fig. 3. Comparison graph of metal 1 contact resistance
(a) N+ active contact resistance
(b) Borderless contact resistance in Kelvin pattern
(c) N+ poly contact resistance
(d) Borderless contact resistance



a) White image without ISP @ 5100 Kelvin deg.

0.65	0.03	0.21	0.23	0.42	0.83	0.89	0.55
0.62	0.22	0.11	0.27	0.11	0.61	0.58	0.48
0.55	0.20	0.18	0.19	0.10	0.75	1.01	0.57
0.43	0.01	0.46	0.37	0.45	1.15	1.19	0.89
0.66	0.25	0.32	0.08	0.30	0.99	1.04	0.71
1.03	0.52	0.33	0.47	0.39	0.32	0.57	0.42
1.31	0.92	0.77	0.76	0.74	0.26	0.10	0.08
1.40	1.16	0.83	0.92	0.84	0.40	0.34	0.41

b) Gr/Gb difference at divided image (unit : %)

Fig. 4. Gr/Gb ratio of whole image which was captured by the 2Mega product of this work.

Fig. 5. Captured sample image of this work.